



ADMINISTRATIVE PROCESS CONTROL PROCEDURE

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Document Name:	Procuring Printed Circuit Boards		
Document Number:	PR0010	Rev: I (12-4-18)	Date: 10-31-08
Controlling Dept:	Quality		
Changes:	<i>PR0010-1,-2,-3 obsolete; SM0013&-1 not referenced; 5.22 remove laminates list</i>		

1.0 PURPOSE

1.1 This procedure provides the technical requirements that must appear on quotes before sending to printed wiring board fabricators.

2.0 SCOPE

2.1 All quotes to be submitted to PWB fabricators shall comply with this appendix.

3.0 ASSOCIATED MATERIALS

3.6 IPC 600 Acceptability of Printed Boards

3.7 IPC 1601 Printed Board Handling and Storage Guidelines

4.0 DEFINITIONS

4.1 **RFQ:** Request for Quote

4.2 **BOM:** Bill of Material

4.3 **VPR:** Vendor Problem Report

4.4 **NCNR:** Non-Consumable, Non-Returnable

4.5 **PCB:** Printed Circuit Board

4.6 **FEI:** Federal Electronics, Inc.

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5.0 PROCEDURE

The requirements listed below shall apply to all PCB RFQ's and PO's submitted to board fabricators unless otherwise stated:

TECHNICAL REQUIREMENTS FOR PCB FABRICATORS

- 5.1** Supplier to provide C of C indicating that they follow the guidelines and testing requirements identified in the IPC 600 latest revision specification.
- 5.2** A 0.500" scored break-away is required on 4 sides.
- 5.3** When scoring is not applicable, i.e. when components overhang or are within 0.050" of edge, boards are odd shapes, etc., 0.500" rails are still required with a routed procedure.
- 5.4** The route shall be .100" width.
- 5.5** If routing is used then connecting tabs shall be of the low stress "mouse bite" breakaway type with holes drilled along the break lines of the boards (1 on each side if connecting 2 boards).
- 5.6** Rails shall have thieving and fiducials added to both ends of the two rails.
- 5.7** Rails are required whenever any SMT or fiducial pads are within 3.0mm from conveyer edge of the PCB.
- 5.8** Fiducials shall be 1.0mm diameter with a solder mask clearance of 2.0mm from center of fiducial.
- 5.9** Supplier must notify Federal Electronics if fiducials are not present.
- 5.10** If size becomes an issue, then the rails may be reduced to 0.250".
- 5.11** 0.125" non-plated tooling holes need to be added to the rails and spaced 0.250" from the board edges.
- 5.12** Maximum Panel size for our Pick and Place equipment is 20.0" x 17.1". Panel size is not to exceed the above dimensions.
- 5.13** Fab supplier to provide panelization scheme for best fit and cost for their process and provide the Gerber files after FEI approval.
- 5.14** Maximum board width is 12", length can be as long as 20".
- 5.15** Package required: Per suggested array.
- 5.16** All fabs shall be tested electrically for continuity and shorts per IPC-D-356 (current version).
- 5.17** Verify gerber data and compare with provided net list. Advise Federal Electronics immediately if any discrepancies are found between the gerber data and net list.
- 5.18** All fabs shall pass a solderability test per J-STD-003 at time of manufacture.
- 5.19** One solder sample shall accompany each shipment, including a Certificate of Conformance (CofC).
- 5.20** A solder array sample is required for the initial delivery of fab orders and for first shipments of revision or design changes.
- 5.21** When quoting or fabricating "no-lead" boards, RoHS compliant shall be required.
- 5.22** Laminates shall be per Customer documentation.
- 5.23** Finish: Immersion Gold unless otherwise specified on Customer documentation.
- 5.24** Solder mask shall be green LPI over bare copper or equivalent unless otherwise specified on customer documentation.
- 5.25** Silk screen ink shall be white non conductive epoxy or equivalent unless otherwise specified on customer documentation.
- 5.26** Other info as required.
- 5.27** PCB Fab houses must comply with IPC-1710A, current version.
- 5.28** Boards shall be packed (dry packed) per IPC-1601, current revision.

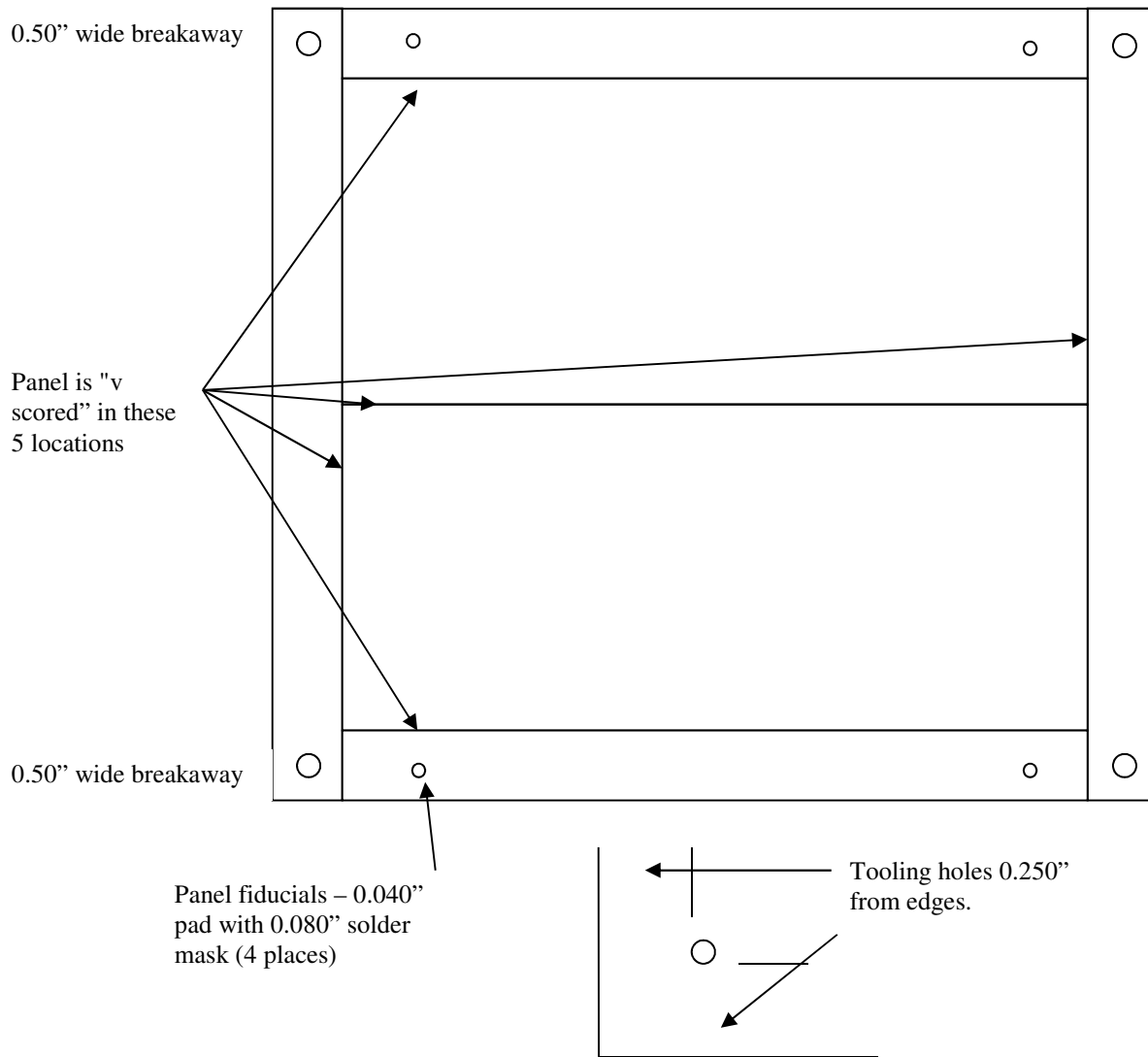
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Federal Electronics Fab Requirements**

The diagram below is a generic panel drawing with fiducial locations and sizes. Rails should have thieving. Thieving is required on external layers and allowed on internal layers. A staggered hatch pattern such as 0.050" circles on 0.075" centers is acceptable.

Please add 0.125" non-plated tooling holes exactly 0.250" from each edge and fiducials another 0.500" towards board center.

Note: If scoring is not applicable, i.e. components are within 0.050" of edge of board, a 0.100" route is recommended.

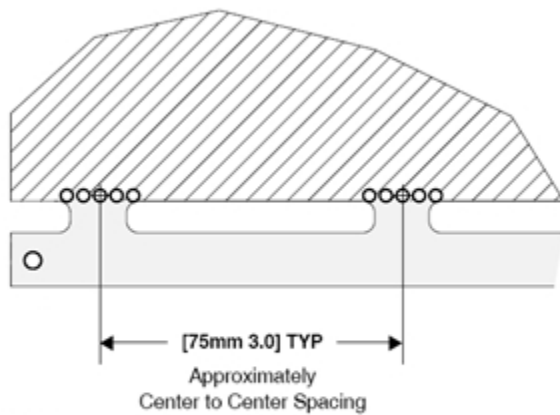
Drawing 1



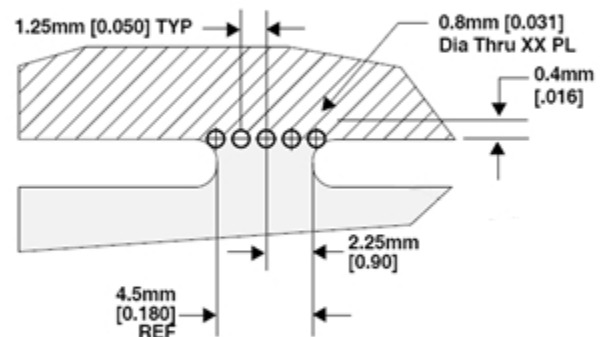
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Drawing 2
Typical Breakaway Design For Routed Boards

Breakaways (Dimension shown are an example only - deviation is allowed)



Depending on PWB
Outline Design



Detail of Breakaway

LOW STRESS (MOUSE BITE) BREAKAWAY

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Additional PCB Info**

Please see the following charts:

Here are the copper to edge/soldermask openings required to avoid exposed Copper. (typical values) for associated part thickness.

PCB Thickness	Copper & Solder Mask Clearance
0.51mm [0.020"]	0.15mm [0.006"]
0.79mm [0.031"]	0.15mm [0.006"]
1.60mm [0.062"]	0.25mm [0.010"]
2.00mm [0.078"]	0.32mm [0.012"]
2.40mm [0.093"]	0.38mm [0.015"]
3.18mm [0.125"]	0.46mm [0.018"]

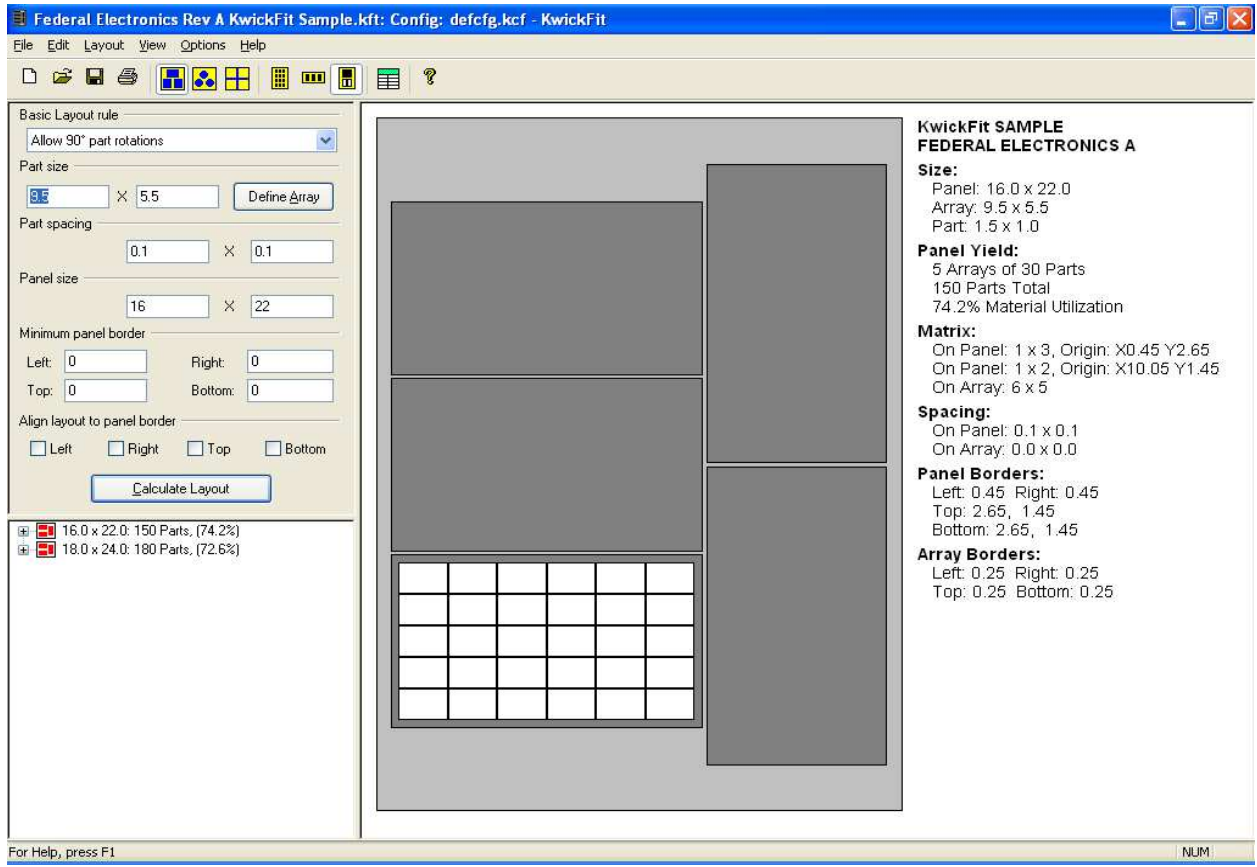
Here is the web thickness (remaining material after score) that should be used. This will avoid problems with removing rails after score:

PCB Thickness	Web Thickness
0.51mm [0.020"]	0.20mm [0.008"]
0.79mm [0.031"]	0.23mm [0.009"]
1.60mm [0.062"]	0.38mm [0.015"]
2.00mm [0.078"]	0.41mm [0.016"]
2.40mm [0.093"]	0.46mm [0.023"]
3.18mm [0.125"]	0.51mm [0.024"]

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Federal Electronics
Bare Substrate Electrical Test

All fabs to be 100% tested using a supplied Net List. Testing should comply with the latest rev of IPC-D-356(Bare Substrate Electrical Test Format). Absolutely no “Golden Board” testing is permitted. If a Net List is not provided, please inform purchasing.



**FEDERAL ELECTRONICS
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VENDOR RECOMMENDED MODIFICATION FORM
Printed Circuit Board Fabrication**

DATE: ____/____/____
VENDOR NAME: _____
VENDOR CONTACT: _____
TEL/EXT NUMBER: _____
PART ID/REV: _____
PART DESCRIPTION: _____
VENDOR RECOMMENDED MODIFICATION(S): _____ _____ _____ _____
POTENTIAL SAVINGS PER BOARD BASED ON THESE MODIFICATIONS: \$ _____



FEDERAL ELECTRONICS APPROVAL SIGNATURES:

MATERIALS: _____ DATE: ____/____/____

ENGINEERING: _____ DATE: ____/____/____

QUALITY: _____ DATE: ____/____/____

COMMENTS: _____

